Design of High-Speed Master–Slave D-Type Flip-Flop in InP DHBT Technology

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***Abstract*—In this paper, we present some design problems of high-speed master–slave D-type flip-flop (MS D-FF). Essential to the long-haul optical-fiber communication systems, this circuit is critical since it operates at the highest clock frequency for a given bit rate. We discuss specific aspects of electrical design of such a circuit and underline some important points for the layout of gigabit circuits. In particular, we tackle the problem of ringing, which can appear in emitter–follower structures using the fast transistors necessary for high-speed operation. We have pointed out also some difficulties of circuit layout, particularly certain connections that can cause serious ill functioning. The MS D-FF was fabricated in our self-aligned InP double heterojunction-bipolar-transistor technology. On-wafer characterizations at 40 Gb/s show 75% horizontal and 68% vertical eye opening.**

***Index Terms*—Bipolar integrated circuits, flip-flops, indium compounds, SONET, very high-speed integrated circuits.**

I. Introduction

THE important increase of communication services, particularly Internet traffic, needs to be supported by the development of adequate networks. Optical fiber, with its huge transmission capacities, is the dominant technology for long-haul communications.

To achieve high-speed transmissions, several data tributaries have to be combined. Time-division multiplexing (TDM) assigns individual data channels to time slots in a higher speed stream. As number of multiplexed channels increases, the bit period get shorter. Systems with 10 Gb/s (corresponding to the synchronous division hierarchy (SDH) STM-64 European standard and SONET OC-192 North American standard) are now in commercial use. Due to the hierarchical nature of these standards, with multiplication by four of the transmission bit rate when passing to the next level, the next single channel to be implemented is 40 Gb/s. Progresses in high-speed microelectronics have already permitted to set up 40-Gb/s electrical time-division multiplexing (ETDM) experiments, while first 80-Gb/s circuits begin to be evaluated.

A combination of ETDM and dense wavelength division multiplex (DWDM) results in multiterabit transmission capacities [1]. For example, in [2], a 5.12-Tbit/s transmission consisting of a combination of 128 wavelengths modulated at 40 Gb/s each over 300 km has been reported.

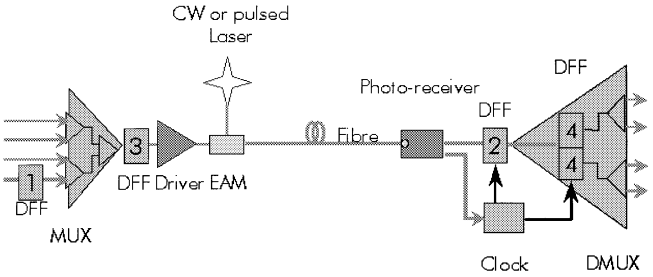

Fig. 1. ETDM synoptic with DFF role emphasized: 1) as a delay, 2) as a decision circuit, 3) as a reshaper, and 4) as a DMUX.

Different very high-speed integrated circuits (VHSICs) are necessary to realize ETDM systems. Each of them presents specific requirements and is a challenging design task at 40–80 Gb/s.

D-type flip-flop (D-FF) is a key electronic component in transmission systems, particularly for the physical (PHY) layer (Fig. 1). It is used to synchronize and/or delay data with respect to the clock, but also as a reshaper and, at the receiving end, as a decision circuit. This decision circuit is at the core of demultiplexing circuits, which can be realized (at the expense of phase margin (PM) and SNR) with two D-FF operating at half the bit rate, controlled by the clock and its opposite. It can also be used for more complex functions such as eye-diagram monitoring [3]. High-speed D-FF and decision circuits have been fabricated in different technologies, i.e., GaAs heterojunction bipolar transistor (HBT) [4], InP HBT [5], [6], InP high electron-mobility transistor (HEMT) [7].

The difficulty of this circuit, compared to other composing the ETDM systems, consists of its high clock rate. It actually operates at a clock rate equal to the bit rate (to be compared with the MUX and DMUX circuits, which operate at a clock frequency equal to half the bit rate).

In this paper, we present the design of a D-FF circuit with a particular focus on electrical level optimization and layout aspects. This circuit was fabricated in InP double heterojunction bipolar transistor (DHBT) technology and measured at 40 Gb/s.

This paper is organized as follows. In Section II, we briefly present the InP HBT technology used for circuit fabrication. In Section III, we discuss various aspects of circuit design. Section IV is devoted to layout problems. Finally, experimental results are shown in Section V.

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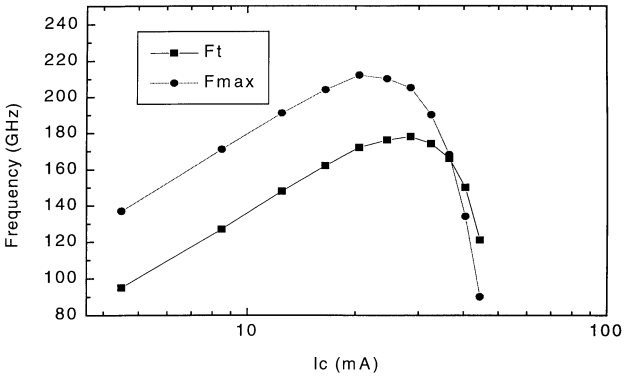

Fig. 2. Measured F_t and $F_{\max}$ (Mason's gain) for a $10 \times 1.5\ \mu\text{m}^2$ device.

II. Technology

The circuit we present has been fabricated in an InP DHBT technology, developed within the OPTO+ Laboratory, Marcoussis, France. The baseline technology has been presented in detail in [8] and [9].

The InP–InGaAs self-aligned transistors have been fabricated on a chemical beam epitaxy (CBE)-grown epitaxial structure. The use of a graded base eases the HBT scaling and permits emitter width reduction without current-gain degradation. A high breakdown voltage ($\text{BV}_{\text{CE0}} > 6$ V) is the result of the double heterojunction structure.

In order to improve the frequency characteristics of the devices, it is important to minimize both the base resistance R_B and the base–collector junction capacitance C_{BC}. The general approach consists of decreasing the dimensions, but then parasitic effects tend to dominate. For emitter lengths smaller than 10 μm, a self-aligned base-pad isolation process has been introduced. It reduces the parasitic base–collector effects. Thus, high performances can be maintained even for small transistor length: F_t above 150 GHz is achieved for currents in the 2–6-mA range for $1.5 \times 2\ \mu\text{m}^2$ devices. Such a type of transistor can be suitably used for very low-power high-frequency applications.

On-wafer S-parameter measurements were performed up to 65 GHz with V_{CE} of 1.6 V. 170 GHz F_t and 210 GHz $F_{\max}$ are currently obtained on circuit-oriented devices at a current density of 2.2 $\text{mA}/\mu\text{m}^2$. In Fig. 2, measured F_t and $F_{\max}$ (Mason's gain) are presented in function of I_c for a $10 \times 1.5\ \mu\text{m}^2$ device.

Three Ti/Au interconnection levels, TaN resistors, metal–insulator–metal (MIM) capacitors and spiral inductors are available for the designer; the three interconnection levels are useful to optimize the circuit layout.

III. Circuit Design

Detailed time-domain simulations are necessary to assess correct operation of VHSICs. As full-custom design is needed, precise transistor models for various geometries are essential for electrical simulation. Passive elements should also be modeled in the adequate frequency range.

A. Device Modeling

The nonlinear Gummel–Poon (GP) model is widely used for bipolar transistors. Attractive aspects of this model are its simplicity and general availability. Additionally, the limited number of parameters is an advantage in parameter-extraction procedures. Unfortunately, the GP model is not able to predict with high accuracy some of the following specific InP DHBT features [9]:

- current dependence of τ_f due to electric-field profile modulation;
- voltage dependence of τ_f due to intervalley scattering;
- exponential dependence of C_{bc} in high-current regime due to electron accumulation;
- heterojunction-specific "saturation" static regime so that access resistances are not overestimated.

As shown in [10], it is possible to adapt the GP model to main DHBT PHY features by twisting the original meaning of parameters. This approach was used for the presented design.

B. Design Optimization

Transistors Sizing: As for all the VHSICs, the design of the D-FF circuit is full custom. Individual transistor geometries have to be adjusted to reach optimal circuit performances. The base resistance R_b and base–collector capacitance C_{BC} play a leading role in the propagation delay time; thus, it is necessary to lower the $R_b \times C_{\text{BC}}$ product. This can be done by choosing the smallest emitter width allowed by the technology and providing the appropriate current density in the transistor.

In our design, transistors with emitter dimensions $10 \times 2\ \mu\text{m}^2$ were used. At 1 $\text{mA}/\mu\text{m}^2$ current density, these transistors have $F_t = 140$ GHz and $F_{\max} = 150$ GHz.

Emitter–Follower (EF) Optimization: To achieve a correct operation at the highest possible speed, emitter-coupled logic (ECL) or E^2CL architectures are used. The EF structures allow obtaining better matching between common-mode logic (CML) stages. However, these structures, especially realized with rapid transistors, must be carefully designed to avoid excessive oscillations. These oscillations are caused by the combination of a negative real part of EF impedance and input capacitance. Damping techniques with resistors can be used, but at a cost of increasing the rise and fall times. The availability of precise transistor models is crucial for optimization of this stage. In fact, different τ and C_{BC} model combinations can reproduce similar transistor speed, while predicting a completely different effect on oscillations.

Electrical Simulations: To make simulations more reliable in the context of nonperfect modeling, some additional computer-aided design (CAD) modules were developed. The choice of an operating region can be based on the synthetic information presented in Fig. 3, where the frequency performances (F_t) were overlaid on dc characteristics. The voltage breakdown line is also shown. After a transient simulation, it is possible to visualize the duty cycle for each transistor. It can be presented together with additional characteristics like dc characteristics, iso-Ft, or iso-power lines. In Fig. 4, duty cycles for CML, ECL, and E^2CL pairs are presented. These curves compared with iso-Ft lines in Fig. 3 indicate that ECL and E^2CL pairs operate in more favorable conditions as far as frequency performances are concerned. The rise and fall times for the three previously mentioned pairs are presented in Fig. 5. It can be noted that ECL

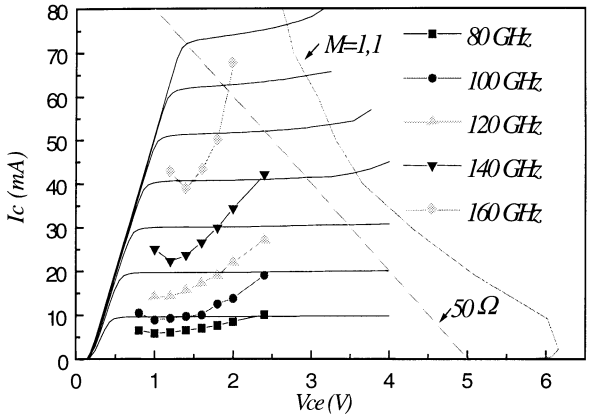

Fig. 3. $I_c(V_{ce})$ characteristics with iso-Ft curves and breakdown voltage line.

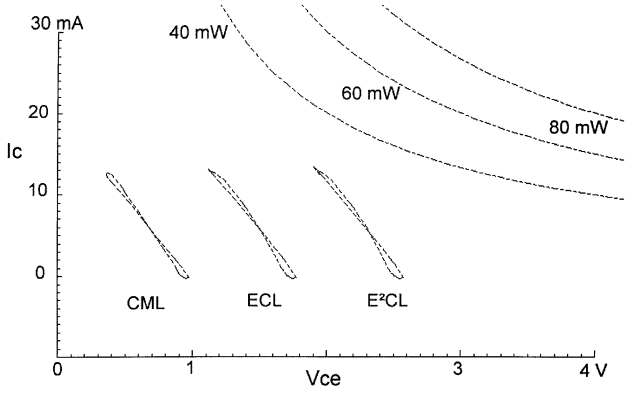

Fig. 4. Duty cycles for CML, ECL, and E^2CL.

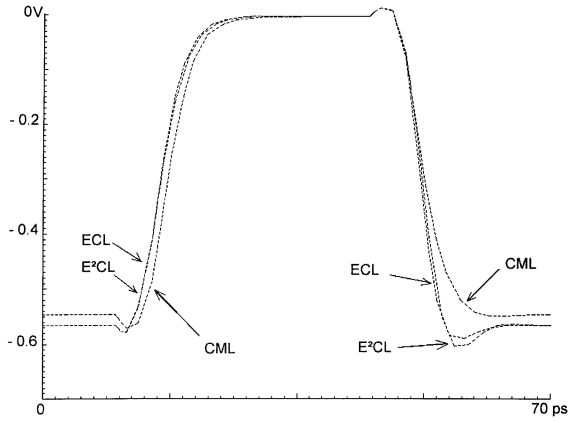

Fig. 5. Pulse simulation for CML, ECL, and E^2CL.

and E^2CL curves are similar, while there are differences in the delay and fall times for CML pair simulation.

Final simulation of circuit operation is obtained with a pseudorandom source representing the input signal. Lengthy transient simulations are necessary to evaluate the time jitter. A simulator from the SPICE family has been used.

C. Architecture and Simulation Results

The precise specifications of the D-FF depend on its role in the system. When used as a re-timer/re-shaper, jitter, rise, and fall times are more important than sensitivity. At the receiving end, sensitivity is a key parameter for its consequences in the system design. For eye-diagram monitoring, both PM and sensitivity are the more important parameters.

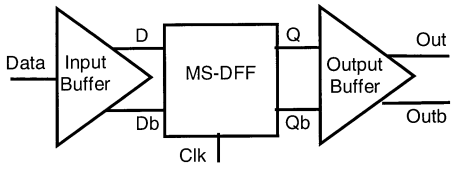

Fig. 6. DFF block diagram.

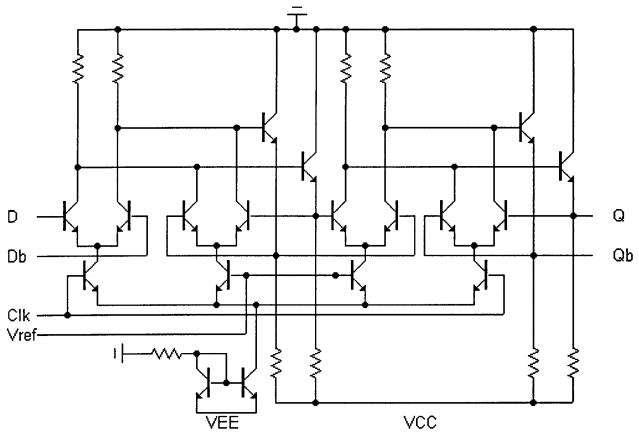

Fig. 7. DFF core electrical scheme.

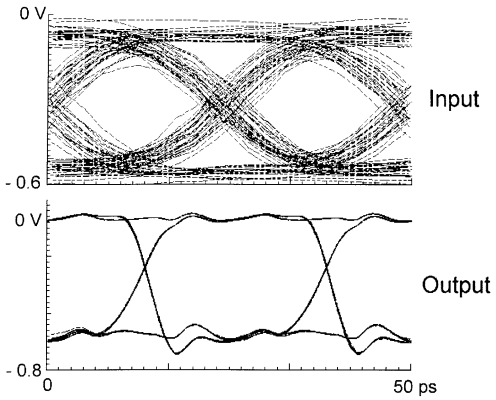

Fig. 8. DFF simulation with 40 Gb/s. Real (*top*) input and (*bottom*) output.

The MS D-FF circuit consists of an input buffer, which is decisive for sensitivity, the circuit core that realizes the D-FF function, and an output buffer. In Fig. 6, the D-FF block diagram is presented. DFF cores with ECL and E^2CL structures have been designed. Similar bit-rate operation has been obtained, while the power consumption of the ECL core architecture was 460 mW instead of 540 mW with the E^2CL structure. The electrical scheme of the ECL D-FF core is presented in Fig. 7.

DFF simulation results are presented in Fig. 8. The input signal (40 Gb/s) is the one registered from the measurement setup. A sinusoidal ideal clock signal has been applied. In Fig. 9, the decision operation has been simulated. The 50-Gb/s input is the registered signal issued from voluntarily degraded MUX operation.

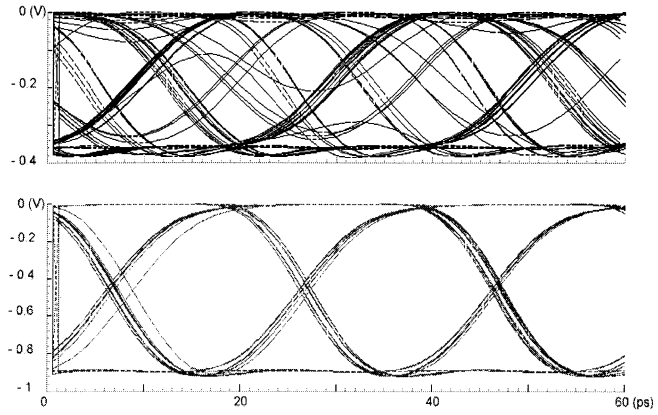

Fig. 9. DFF decision operation at 50 Gb/s. (*top*) Input and (*bottom*) output.

IV. Layout Problems

As the complexity and the circuit speed increase, the performances are limited by the parasitic elements introduced during the layout process, such as crossing capacitances, imperfect ground references, long transmission lines, etc. [11], [12]. Qualitative rules are applied to reduce the degradation due to these parasitic elements: crossing areas between the interconnection levels are minimized and inductive voltage-supply metallization avoided as far as possible. Due to circuit complexity, it is not possible to maximally shorten all connections. For a given circuit architecture, critical connections are identified and shortened as much as possible.

Furthermore, full-custom layout techniques (symmetrization, parasitic extraction) were developed and utilized throughout the design.

A. Layout Parasitic Extraction

As presented in [13], home-developed layout extraction tools have been used in order to simulate the most critical layout parasitic effects. Our CAD tools permit the extraction and the post-simulation of each interconnection line (coplanar or microstrip), which is considered as critical. However, the complexity of this layout does not allow the simulation of the circuit with all parasitic elements simultaneously taken into account.

B. Influence of Parasitics in EF Connection

In this section, we show how degradation caused by ground metallization parasitics can become dominating and have disastrous effects upon the circuit performance.

The first version of the D-FF circuit was simulated, taking into account the crossing capacitances and interconnection considered as critical [see Fig. 10(a)]. As mentioned before, it is not possible to systematically take into account all parasitic elements. In our case, one of the connections (the EF pair at the clock input connection to ground, shown in Fig. 11) was badly dimensioned. The metallization was too narrow. The parasitic inductance of this interconnection caused voltage fluctuations resulting in closing of the eye diagram beginning at 30 Gb/s. This effect was confirmed by simulation as presented in Fig. 10(b).

This example shows the importance of the layout phase and the necessity of human expertise to properly choose the critical

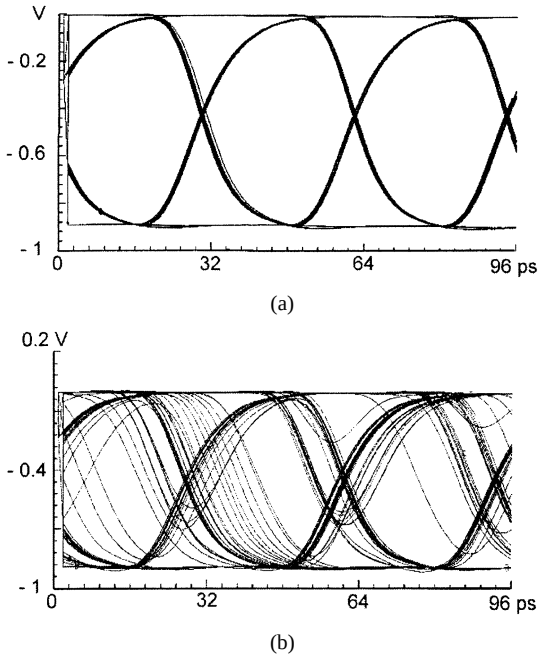

Fig. 10. (a) D-FF simulation at 40 Gb/s with main parasitic effects. (b) D-FF simulation at 32.5 Gb/s with parasitic connection to ground.

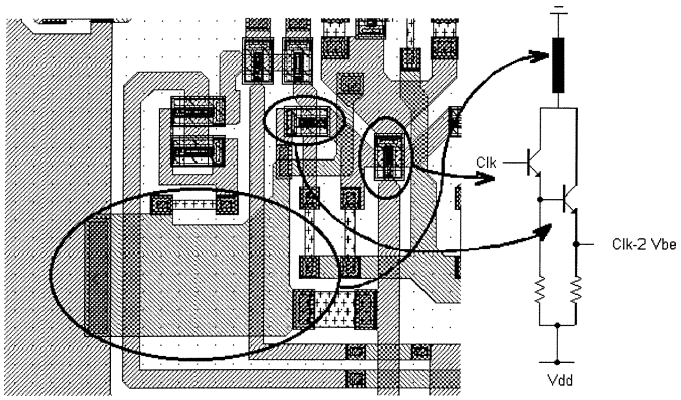

Fig. 11. Badly dimensioned EF connection to ground.

parts to be back-annotated for simulation, as automated full parasitic extraction is currently not possible for VHSICs.

The layout was corrected and the microphotograph of the fabricated chip is shown in Fig. 12. The chip dimensions are 1.4×1.2 mm^2.

V. Experimental Results

The measurement setup is composed as follows. A 20-Gb/s pseudorandom bit pattern and its complementary are available. One data stream is delayed and is multiplexed with the other using a 40-Gb/s MUX. The pseudorandom bit pattern generator (PRBG) and MUX are clocked by the same frequency synthesizer. This synthesizer is synchronized with a low phase-noise frequency synthesizer, which provides the circuit's clock signal. A 50-GHz-sampling oscilloscope has been used.

50-Ω on-chip output and input resistances provide an efficient impedance matching for testing and packaging. Less than -12 dB of signal reflection at the input and less than -8 dB at the output were measured up to 65 GHz (cf. Fig. 13).

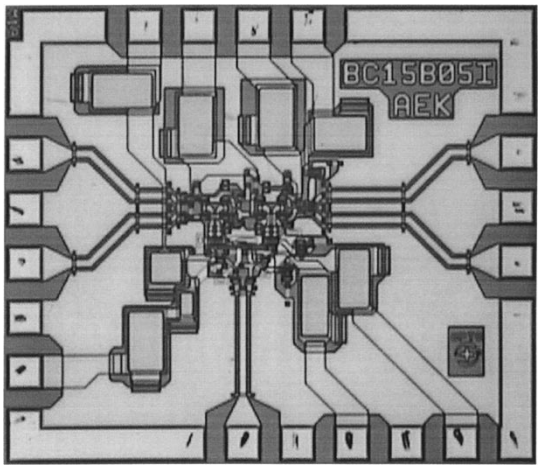

Fig. 12. Microphotograph of D-FF layout.

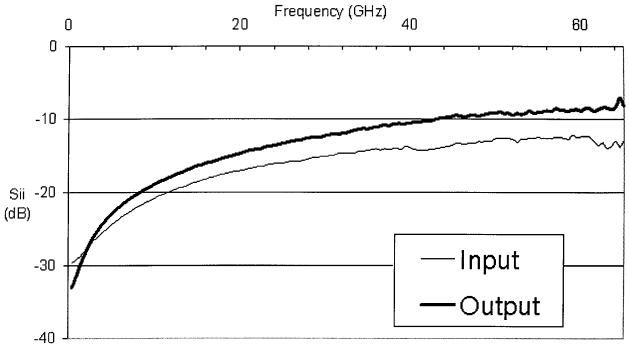

Fig. 13. Signal reflection measurement at the input and output of the D-FF circuit.

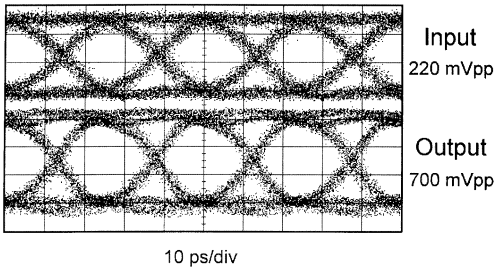

Fig. 14. Eye diagram at 40 Gb/s. (*top*) Input and (*bottom*) output.

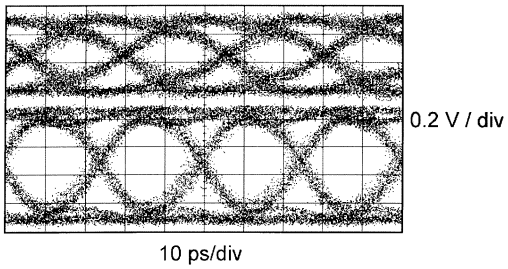

Fig. 15. DFF regenerating capabilities at 40 Gb/s. (*top*) Input and (*bottom*) output.

In Fig. 14, the measurement results at 40 Gb/s are presented. The 700-mV_{pp} output signal presents 1.1-ps rms time jitter. The input signal rms jitter is 1.43 ps. The horizontal eye opening is 75%, while the vertical is 68%. The rise and fall times (20%–80%) are approximately 8 ps. Roughly estimated PM is 12 ps. This value compared to time bit (25 ps) gives 173°. A PM evaluation taking into account the peak-to-peak input jitter $(\text{margin(ps)}/(\text{timebit - jitter)(ps)} \times 360^{\circ})$ would give 263°.

In Fig. 15, the measured regenerating capabilities of D-FF are shown. A voluntarily degraded input is correctly restored by the D-FF.

VI. Conclusion

We have presented problems related to the design of high-speed D-FF circuits. In particular, we discussed the problem of ringing, which can appear in EF structures using the rapid transistors necessary for high-speed operation. We pointed out also some difficulties of circuit layout, and especially how certain connections can cause serious dysfunction of the circuit. An MS D-FF has been fabricated in InP HBT technology and characterized on-wafer. At 40 Gb/s, this circuit presents excellent regenerating properties, a good PM, and low time jitter.

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Habiba Ouslimani, photograph and biography not available at time of publication.

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In 1978, he joined Centre National d'Etudes des Télécommunications (CNET) (now France Telecom Research and Development), where he was involved in digital-signal-processing developments, based particularly on Si- and III–V charge-coupled devices (CCDs). Since 1985, he has been in charge of CAD support and developments for the laboratory, particularly for HBT VHSIC design. Since 1995, he has led a department in charge of developments in HBT technology and circuits design. This department is now part of OPTO+, Alcatel Research and Innovation, Marcoussis, France. His main interests are VHSIC CAD methodology and III–V circuits for very high bit-rate optical communications.